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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,723	DATTA ROY ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/12/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 9, 10, 11, 12, 13, 14 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartung et al, U.S. Patent No: 5,920,709 **[herein after Hartung]**.

3. ***As per Claim 1***, Hartung teaches a method for detecting whether an IDE drive **[see Fig. 13, element 40 – also see Col. 1, Lines 41-44**, *"IDE devices such a magnetic tape drives and hard drives"***]** is connected to an drive electronics channel within a computer **[see Fig. 6, element 60D]**, comprising:

> (a) Writing data to a drive head register destination for the IDE drive **[Col. 1, Lines 55-60, -- All information regarding the IDE drive is written into the registers]**
>
> (b) In response to writing the data to the drive head register destination, reading the drive head register destination and detecting whether the data read from the drive head register destination matches the data written to the drive head register destination **[Col. 11, Lines 37-42]**
>
> (d) In response to the data read from the drive head register destination not matching the data written to the drive head register destination, returning that the IDE drive is not connected to an intelligent drive electronics channel **[see Col. 11, Lines 42-55]**
>
> (e) Reading a status register **[see Col. 9 Line 64 – Col. 10, Line 5]** destination for the IDE drive **[Col. 1, Lines 49-55]**
>
> (f) Determining whether the IDE drive is connected based on a value read from the status register destination **[Col. 11, Lines 48-52]**.

4. ***As per Claim 14***, Hartung teaches a computer program product having control logic stored therein for causing a computer to detect whether an IDE drive **[see Fig. 13, element 40 – also see Col.**

1, Lines 41-44, *"IDE devices such a magnetic tape drives and hard drives"***]** is connected to an intelligent drive electronics channel within the computer **[see Fig. 6, element 60D]**, said control logic comprising means for causing the computer to:

(a) Establish a drive selection value for each IDE drive wherein each IDE drive comprises at least one of a master IDE device and a slave IDE device **[see Col. 5, Lines 25-30]**

(b) Remaining limitations are similar to those addressed in rejection of Claim 1. Please refer to the above provided citations.

5. ***As per Claim 19***, Hartung teaches a computer system for detecting whether an IDE drive **[see Fig. 13, element 40 – also see Col. 1, Lines 41-44**, *"IDE devices such a magnetic tape drives and hard drives"***]** is connected to an intelligent drive electronics channel within the computer system **[see Fig. 6, element 60D]**, the computer system comprising:

(a) Processor **[see Fig. 6, element 62, "Main System Microprocessor"]** coupled to a memory **[see Fig. 6, element 67, "RAM"** – *as can be seen, element 62 is coupled to 67***]**

(b) At least one bus **[see Fig. 6, element 66]** coupled to the processor and capable of hosting at least one IDE drive via an intelligent drive electronics channel **[see elements 60A-60D**, *either directly or indirectly (through ISA Bus), four IDE bus are connected to Main System Microprocessor (62)***]**

(c) Basic input/output system program capable of being executed on the processor and when executed on the processor **[see Col. 10, Lines 6-13]** operative to:

(d) Remaining limitations are similar to those addressed in rejection of Claim 1. Please refer to the above provided citations.

6. ***As per Claim 2,*** Hartung teaches a method wherein determining whether the IDE drive is connected comprises:

(a) Detecting whether data read from the status register destination has a first predefined value **[see Col. 11, Lines 42-45** – *whether registers have a string of hexadecimal "F" values***]**

(b) Upon the data read from the status register destination not having the first predefined value, returning that the IDE drive is connected to the intelligent drive electronic channel **[Col. 11, Lines 48-52]**

7. ***As per Claim 4***, Hartung teaches a method further comprising:

(a) Prior to writing data to a drive head register destination for the IDE drive, establishing a drive selection value for each IDE drive **[Col. 10, Lines 59-66]**

(b) Selecting the IDE drive for detection by writing a drive selection value to the drive head register destination **[Col. 12, Lines 48-55]**

8. ***As per Claim 9***, Hartung teaches a method wherein two IDE drives may be connected per intelligent drive electronics channel and wherein a one of the IDE drives comprises a master drive and a one of the IDE drives comprises a slave drive **[Col. 5, Lines 11-18]**

9. ***As per Claim 10,*** Hartung teaches a method wherein the drive selection value represents at least one of master drive and the slave drive **[see Col. 5, Lines 25-30]**

10. ***As per Claim 11***, Hartung teaches a method further comprising, prior to reading a status register destination, resetting the computer **[Col. 6, Lines 6-13]**

11. ***As per Claim 12,*** Hartung teaches a method wherein resetting the computer comprises executing at least one of the following: Power on reset of the computer; hardware reset; execute drive diagnostics command; software reset and drive reset **[Col. 6, Lines 25-28, "Perform Device Diagnostic"** – *Though Hartung teaches other limitations as well, the claim only requires "at least one" of the list*]

12. ***As per Claim 13,*** Hartung teaches a method wherein the IDE drive comprises at least one of the following: hard disk drive, floppy drive, CD ROM disk drive and tape drive **[see Fig. 13, element 40 – also see Col. 1, Lines 41-44**, *"IDE devices such a magnetic tape drives and hard drives"*]

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 5, 6, 7, 8, 16, 17, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartung and further in view of Nakamura U.S. Patent No: 7,046,519 **[herein after Nakamura]**.

15. ***As per Claims 5, 16 and 21***, Hartung teaches all the limitations of Claims 2, 14 and 19. Hartung fails to teach a system wherein the system uses cylinder low register destination and cylinder high register destination for the IDE drive. Nakamura teaches the above limitation of having a cylinder low register and cylinder high register **[see Col. 8, Lines 52-64]**.

One of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the teachings of Hartung with that of Nakamura in order to take advantage of exchanging data between the small communication card and the personal computer using the register group used in a PC card interface **[Col. 9, Lines 45-50]**

16. ***As per Claim 6 and 17***, Hartung as modified by Nakamura teaches a system wherein the IDE drive is connected to the intelligent drive electronics channel implements a packet command feature set **[see Fig. 6, element 60D]**

17. ***As per Claim 7***, Hartung as modified by Nakamura teaches a system wherein in response to the data read from cylinder low register destination and the cylinder high register destination not matching the predefined signature, returning the IDE drive is not connected to an intelligent drive electronic channel **[see Col. 11, Lines 42-45 –** *whether registers have a string of hexadecimal "F" values and if it doesn't, concluding that the IDE device is not connected***]**

18. ***As per Claim 8 and 18***, Hartung as modified by Nakamura teaches a method wherein the predefined signature comprises a second predefined value of the cylinder high register destination and a third predefined value of the cylinder low register destination [**Col. 8, Lines 52-64**].

Response to Arguments

19. Applicant's arguments filed 4/16/2007 have been fully considered but they are not persuasive.

Applicant argues that prior art of record fails to teach:

(a) "...In response to the data read from the drive head register destination not matching the data written to the drive head register destination, return that the IDE drive is not connected to an intelligent drive electronic channel"

(b) "Writing data to a drive head register destination for the IDE drive..."

(c) "Cylinder low register and cylinder high register" and further the combination of the secondary reference with Hartung.

20. As per Argument (a), **Examiner disagrees**. Applicant argues that Hartung discloses that when the nest drive sees a string of hexadecimal "F" values on any of the IDE buses, nest drive realizes that no device is connected to such bus 63. In other words, Hartung teaches that if the value the nest drive sees on the IDE bus matches a string of hexadecimal "F" values, then the nest drive realizes that no device is connected to the bus. However, it seems to the Examiner that the Applicant is solely focusing on isolated teachings of Hartung without understanding the overall invention of Hartung in order to support his argument. It should noted that Hartung teaches a system wherein connection of the IDE device to the system is determined by the response over the IDE bus through the various hexadecimal values that are broadcast over the bus system. In Hartung system, it is determined that the IDE device is connected to the system when nest driver sees a hexadecimal value "EB14" being returned via any bus 63 **[see Col. 11, Lines 48-52]**. Therefore, it is conclusive that when the nest driver does not see the "EB14" hexadecimal value it is consequently determined that the IDE device is not connected to the system. Hartung's system further has other values that can be broadcasted over the bus system including a string of "F" values that confirm that the IDE device is not connected and further "Abort" command determining that the device connected to that bus is not an IDE/ATAPI device **[see Col. 11, Lines 37-48]**. Therefore, since the other two broadcast commands outside of "EB14" indicate a non-IDE device connection state, Examiner submits that non-matching of "EB14" to realize that no IDE device is connected is sufficient for the claim language currently presented.

21. As per Argument (b), **Examiner disagrees**. Applicant argues that prior art fails to disclose "writing data to a drive head destination for the IDE drive" and further "in response to writing the data to the drive head register destination, reading the drive head register destination to determine whether the IDE device is connected." Hartung teaches in previously cited section discloses the nest having a "set of registers for storing information indicative of a current state of the IDE bus." [See Col. 1, lines 49-55]. Further, Hartung teaches a system wherein anytime the state changes with respect to IDE device being inserted or removed, the said set of registers are updated with appropriate hexadecimal values indicating the said state. Hartung further discloses monitoring the set of registers and the IDE busses in order to determine whether or not IDE device is connected to the system or not **[see Col. 1, Lines 55-60 – also see Col. 6, Lines 6-23 for detailed elaboration on provided teachings]**.

22. As per Argument (c), **Examiner disagrees**. Applicant argues that essentially outside of teaching similar terms of "cylinder low register" and "cylinder high register," Nakamura does not remotely relate to the environment of determining whether the IDE device is connected or not. However, it should be noted that Hartung as cited above teaches having a set of registers to determine the status of the IDE devices with respect to their connectivity to the system. However, Hartung does not teach a system wherein the said set of registers include cylinder low and high registers as means for storing values. Examiner simply relies on the secondary reference in terms of installing Nakamura's cylinder low and high registers in place of Hartung's set of registers. As Applicant submits in the arguments, Nakamura teaches that parameters may be set in the cylinder low registers and cylinder high registers, among other registers in the PC card ATA standard **[see Nakamura, Col. 6, Lines 62 – Col. 7, Line 4]**. Therefore it should be noted that Nakamura does not need to be in same analogous art of determining whether or not IDE devices are connected considering the Examiner is solely relying on Nakamura to show that the set of registers can be interchanged with Nakamura's cylinder low and high registers for the reasons provided in the motivation of 103.

23. In light of the above response to arguments, Examiner believes that prior art still reads on the claimed invention as currently provided and thus the prosecution of the present application is being made FINAL accordingly.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
6/17/07

KIM HUYNH
SUPERVISORY PATENT EXAMINER

6/19/07